ELECTRONIC CIRCUIT

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001]

The present invention relates to an electronic circuit that is capable of suitably carrying out communications between substrates such as IC (Integrated Circuit) bare chips, and PCBs (Printed Circuit Boards).

DESCRIPTION OF THE RELATED ARTS

[0002]

Downsizing and high performance have been further advanced in recent electronic devices. In line therewith, incorporated LSIs (Large Scale Integration) have been downsized and high speed processing has progressed. As means for achieving downsizing and high-speed processing, it is desirable that entire functions are included in one package, and now generally two types of realization methods exist.

[0003]

As the first method, a system called "system on chip (SoC)" is available, which incorporates the entire system on a single bare chip. This system is made expensive because different process technologies are realized on one bare chip, and the

yield thereof is lowered due to an increase in the chip area.

[0004]

As the second method, a system called "system in package (SiP)" is available, which seals a plurality of bare chips in one package. With this technique, it is expected that separate chips realize functions produced through different processes, wherein the yield per bare chip is increased, and production costs can be made inexpensive. However, since it becomes necessary that different chips are interconnected to each other, three types of connection techniques exist.

[0005]

The first method for interconnection in SiP is a method conventionally using wire bonding. In this case, the number of connections between chips is the same as in a conventional package or less, wherein a problem occurs in the communications bandwidth. In addition, three-dimensional mounting is indispensable when reducing the mounting area, wherein since, in the wire bonding system, it is necessary to make chips smaller that are to be stacked up, it is difficult to form a bus because the mounting area is restricted and major connections are based on one-to-one connection.

[0006]

The second method for interconnection in SiP is a method

by which chips are three-dimensionally mounted, and connections are based on micro bumps. In this method, costs up to face-to-face mounting of two chips are inexpensive. However, as regards mounting of three or more chips, it is necessary to physically produce a communications path passing through a chip itself or a build-up substrate, a so-called "through hole," wherein an exclusive process technology and highly precise processing accuracy are demanded: resulting in an increase in production costs.

[0007]

The third method for interconnection in SiP is a method for three-dimensionally mounting chips and electrically connecting chips by means of capacitive coupling. Although, for face-to-face mounting up to two chips, costs thereof are inexpensive and high-speed communications are possible, transmission efficiency of signals is radically worsened in three or more chips, wherein power consumption is increased.

[0008]

For this reason, it is proposed that communications between chips are carried out by means of an antenna (for example, refer to Patent Document 1).

[Patent Document 1] Japanese Unexamined Patent Application Publication No. H11-68033

[DISCLOSURE OF THE INVENTION]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

[0009]

However, even in the case of using an antenna, where signals are attempted to be transmitted over chips with three or more chips mounted, it is necessary that an electric field generated by the antenna passes through a number of substances whose dielectric constants are different from each other (biased silicon substrate, doped silicon, oxide film, nitride film, etc.), wherein reflection is generated at a boundary phase, resulting in a worsening in transmission efficiency.

[0010]

In view of the above-described problems, it is therefore an object of the present invention to provide an electronic circuit capable of efficiently transmitting signals even in a case where signals are transmitted over substrates with three or more substrates three-dimensionally mounted. The substrates include an IC bare chip and a PCB.

[MEANS FOR SOLVING THE PROBLEMS]

[0011]

An electronic circuit according to the invention comprising a first substrate including a first coil that is formed by wiring on a substrate and a second substrate including

a second coil that is formed by wiring on a substrate at a position corresponding to the first coil, and is inductively coupled to the first coil.

[0012]

In addition, since the first substrate also includes a transmitter circuit for outputting signals to the first coil when transmission digital data changes, power consumption can be reduced.

[0013]

Also, since the second substrate further includes a receiver circuit that connects both ends of the second coil to a predetermined voltage source via resistors, the center voltage of voltage amplitude occurring at both ends of the receiver coil when receiving signals can be made into a voltage value optimal for the signal amplitude.

[0014]

Further, since the first coil is inductively coupled to the second coils of a plurality of second substrates, a bus over three or more substrates can be formed.

[0015]

Still further, since the second substrate also includes a receiver circuit that receives signals only for a predetermined cyclic period, it is possible to increase the SN ratio.

[EFFECT OF THE INVENTION]

[0016]

According to the present invention, it is possible to efficiently transmit signals where signals are transmitted over substrates with three or more substrates three-dimensionally mounted.

[0017]

Also, since communications are carried out by current drive, the electronic circuit according to the present invention can be favorably employed for LSIs, and the like in which low voltage drive is highly demanded.

The present specification includes the contents described in the specification and/or the drawings of Japanese Patent Application No. 2004-037242 which is the basis of priority of the present application.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[0018]

FIG. 1 is a view depicting a configuration of an electronic circuit according to one embodiment of the present invention;

FIG. 2 is a view depicting a detailed configuration of a transmitter circuit and a receiver circuit in the present embodiment;

FIG. 3 is a view depicting waveforms for describing actions

of the embodiment;

FIG. 4A and FIG. 4B are views depicting a configuration of an electronic circuit according to another embodiment of the present invention;

FIG. 5 is a view depicting a configuration of an electronic circuit according to still another embodiment of the present invention; and

FIG. 6 is a view depicting a detailed configuration of a transmitter circuit according to another embodiment of the present invention.

[DESCRIPTION OF REFERENCE SYMBOLS]

[0019]

11 LSI chip

12 Transmitter circuit

13 Transmitter coil

14 Receiver circuit

15 Receiver coil

400, 401 Transmitter/receiver circuits

403 Inductive coupling

410, 411, 412, 420, 421, 422, 423LSI chips

501 Transmitter/receiver circuit

503 Inductive coupling

510, 511, 512 LSI chips

FF Memory element

INV Buffer

NAND NAND circuit

L Coil

T Transistor

Rxclk Receiving clock

Rxdata Receiving data

Txclk Transmission clock

Txdata Transmission data

Vbias Bias voltage

[BEST MODE FOR CARRYING OUT THE INVENTION]

[0020]

Hereinafter, a detailed description is given of preferred embodiments of the present invention with reference to the accompanying drawings.

[0021]

FIG. 1 is a view depicting a configuration of an electronic circuit according to one embodiment of the present invention. The electronic circuit according to the present embodiment is composed of a first LSI chip 11a, a second LSI chip 11b and a third LSI chip 11c. This is an example in which LSI chips are stacked up in three layers and a bus is formed so as to lie across three chips. The first through the third LSI chips

11a, 11b and 11c are vertically stacked up, and the respective chips are fixed to each other with an adhesive agent. The first through the third transmitter coils 13a, 13b and 13c, which are respectively used for transmission, are formed by wiring on the first through the third LSI chips 11a, 11b and 11c, and also, the first through the third receiver coils 15a, 15b and 15c, which are respectively used for receiving, are formed by wiring thereon. These coils are disposed on the first through the third LSI chips 11a, 11b and 11c so that the centers of openings of these three pairs of transmitter and receiver coils 13 and 15 are made coincident with each other. Accordingly, the three pairs of transmitter and receiver coils 13 and 15 form inductive coupling, thereby enabling communications. The first through the third transmitter circuits 12a, 12b and 12c are connected to the first through the third transmitter coils 13a, 13b and 13c respectively, and the first through the third receiver circuits 14a, 14b and 14c are connected to the first through the third receiver coils 15a, 15b and 15c respectively. The transmitter and receiver coils 13 and 15 are three-dimensionally mounted as coils having one or more turns in an area permitted for communications, utilizing a multi-layered wiring of a process technology. A profile best suitable for communications exists in the transmitter and

receiver coils 13 and 15, and it is necessary that they have an optimal number of times of winging, optimal opening, and optimal line width. Generally, the transmitter coils 13 are smaller than the receiver coils 15.

[0022]

FIG. 2 is a view depicting a detailed configuration of a transmitter circuit and a receiver circuit according to the present embodiment. A transmitter circuit 12 according to the present embodiment is composed of a memory element FF, a delay buffer 121, a first transmission buffer INV2, and a second transmission buffer INV3. Reference number L1 denotes a transmitter coil 13. The transmitter circuit 12 takes a transmission clock (synchronization signal) Txclk as an input and transmission data Txdata synchronized therewith. Inputted transmission data Txdata are stored in the memory element FF and are inputted into the first and the second transmission buffers INV2 and INV3. However, it is constructed so that a delay buffer 121 operating as a delay element is provided prior to the first transmission buffer INV2, and a difference is brought about between the input times into the first transmission buffer INV2 and the second transmission buffer INV3. Outputs of the first transmission buffer INV2 and the second transmission buffer INV3 are, respectively, connected to both ends of the

transmitter coil L1. With the construction, only when a change occurs in the transmission data, a current is permitted to flow into the coil L1 only for the period of a signal propagation delay time of the delay buffer 121. In order to make the receiving voltage of the receiver coil 15 maximum and the margin of the receiving timing larger, the drive forces of the first and the second transmission buffers INV2 and INV3 are set so that the current waveform to the transmitter coil L1 is made into a triangular wave.

[0023]

The receiver circuit 14 is composed of transistors T1 through T10, resistors R1 and R2, NAND circuits NAND1 andNAND2, and a receiving buffer INV1; and forms a latched differential amplifier in its entirety. Reference number L2 denotes a receiver coil 15. It takes a receiving clock (synchronization signal) Rxclk externally and outputs receiving data Rxdata. The transistors T2 and T3 constitute a differential pair of the differential amplifier, and receive signals from the receiver coil L2. Both ends of the receiver coil L2, that is connected to the transistors T2 and T3, are connected to a bias voltage Vbias through the resistors R1 and R2, whereby the center voltage of voltage amplitude occurring at both ends of the receiver coil L2 when receiving signals can be made into a voltage value

Vbias optimized for signal amplification. Source terminals of the transistors T2 and T3 are connected to a transistor T1 for generation of tail current source. The source terminal of the transistor T1 is grounded, and a receiving clock Rxclk is inputted into the gate terminal. At the drain side of the transistors T2 and T3, transistors T5 and T8 and transistors T6 and T9, respectively, form an inverter. The two inverters are connected in the form of a loop. Wiring connecting the inverters is inputted into the NAND circuits NAND1 and NAND2, and the NAND circuits NAND1 and NAND2 form latching. Data received by the differential amplifier change values in synchronization with the receiving clock Rxclk inputted into the transistor T1. The values of the receiving signals are picked up as digital data only when the values change due to the NAND circuit NAND1 and NAND2; on the other hand, the values are maintained when no change occurs in the input values. The transistors T7 and T10 are connected to precharge the differential amplifier and to retain the value of latching while the receiving clock Rxclk is L (low). The transistor T4 is connected in order to prevent the value of the receiving data Rxdata from being reversed due to influences of noise generated by the transistors T7 and T10 although no change occurs in the receiving signals from the receiver coil L2.

[0024]

FIG. 3 is a view depicting waveforms for describing actions of the present embodiment. A description is given of an action in a case where data are transmitted from the third transmitter circuit 12c on the third LSI chip 11c depicted in FIG. 1 to the first and the second receiver circuits 14a and 14b on the first and the second LSI chips 11a and 11b existing thereon. The case where data transmission of [... LLHHLL ...] is carried out as transmission data Txdata is described below as an example. The third transmitter circuit 12c on the third LSI chip 11c inputs a transmission clock Txclk and transmission data Txdata synchronized therewith when transmitting a value. First, in a state where L (Low) is inputted as transmission data Txdata, both of the outputs of the first and the second transmission buffers INV2 and INV3 are in a stationary state in which H (High) is maintained. The first and the second receiver circuits 14a and 14b on the first and the second LSI chips 11b and 11c are in a stationary state with L (Low) outputted to the receiving data Rxdata in a state where L (Low) is continuously inputted.

[0025]

In this state, the transmission data Txdata changes from L to H at the time of point A. The signal is taken in the memory element FF at point B, and is immediately inputted into the

second transmission buffer INV3. Here, although the output of the second transmission buffer INV3 is made L, the output of the first transmission buffer INV2 remains H, wherein a current is caused to flow from the first transmission buffer INV2 to the second transmission buffer INV3. After that, the output of the second transmission buffer INV3 becomes H after the delay time of the delay buffer 121, wherein the outputs of the first transmission buffer INV2 and the second transmission buffer INV3 are made into equal potential, and the current stops flowing. At this time, the drive forces of the first and the second transmission buffers INV2 and INV3 are set so that the current waveform becomes a triangular wave as shown at point B of [transmitter coil current].

[0026]

Voltages shown in the [first LSI chip receiver coil voltage] and the [second LSI chip receiver coil voltage] are generated in the receiver coil L2 disposed on the first and the second LSI chips 11a and 11b by changes in the current at points B and C of the [transmitter coil current]. The center voltage of the voltage variation is Vbias. Since the first LSI chip 11a is farther from the third LSI chip 11c than the second LSI chip 11b, the voltage generated is lowered. The changes in voltage are amplified by the latched differential amplifier

and the value is retained by latching, wherein digital data shown at point B of the [first and second LSI chip Rxdata] are brought about.

[0027]

The transmission data Txdata on the third LSI chip 11c keeps H at the point B and does not make any change. In this case, the input into the transmitter coil L1 at point C does not change, and the voltage of the receiver coil L2 on the first and the second LSI chips 11a and 11b does not change, wherein the output data Rxdata are maintained.

[0028]

Where the transmission data Txdata on the third LSI chip 11c shifts from H to L as at point C, the transmission data Txdata are taken in the memory element FF at the point D, and the input into the second transmission buffer INV3 immediately changes from H to L, wherein the output thereof shifts from L to H. At this time, in respect to the output of the first transmission buffer INV2, a change from L to H is delayed by the delay buffer 121, and a current is caused to flow from the second transmission buffer INV3 to the first transmission buffer INV2. After that, the output of the first transmission buffer INV2 becomes H after the delay time of the delay buffer 121, wherein the output voltages of the first transmission buffer

INV2 and the second transmission buffer INV3 are made equal to each other, and the current stops. The drive forces of the first and the second transmission buffers INV2 and INV3 are set so that a series of changes in the transmission current becomes a triangular wave which takes an inverted polarity of the triangular wave at point B as at point D of the [transmitter coil current].

[0029]

Waveforms at point D of the [first LSI chip receiver coil voltage] and [second LSI chip receiver coil voltage] are generated on the receiver coil L2 of the first and the second LSI chips 11a and 11b by a change in the current of the transmitter coil L1 on the third LSI chip 11c. The change in the voltage is amplified by the differential amplifier and converts the same to digital data by latching, whereby digital receiving signals at point D of the [first and second LSI chip Rxdata] are obtained.

[0030]

In the above, a detailed description has been given of an embodiment of the present invention made by the present inventor. However, the present invention is not limited to the above-described embodiment, but may be subjected to various modifications within the scope not departing from the spirit

thereof.

[0031]

For example, one-to-one connection is available instead of bus connection. FIG. 4A shows an example of connection of this case. FIG. 4A is a view obtained by observing a stacked LSI composed of the first through the third LIS chips 410 through 412 from its side. The content of the transmitter and receiver circuit 401 is depicted as a transmitter and receiver circuit 400. The arrow 403 denotes inductive coupling.

[0032]

In addition, multiple-to-multiple connection is also available. FIG. 4B shows an example of connection of this case. FIG. 4B is a view obtained by observing a stacked LSI composed of the first through the fourth LSI chips 420 through 430 from its side. In this case, communications between the first LSI chip 420 and the third LSI chip 422 and communications between the second LSI chip 421 and the fourth LSI chip 423 are carried out on the same horizontal position. That is, a plurality of combinations of transmitter circuits and receiver circuits are independently inductively coupled using the same space. Since inductive coupling is enabled on the same horizontal position, for example, respective communications can be carried out without any leakage by time-sharing, etc.

[0033]

As described above, expansion can be brought about for not only connections in the vertical direction but also connections in the horizontal direction. FIG. 5 shows an example in which the bandwidth is increased by carrying out communications in parallel. FIG. 5 is a view obtained by observing a stacked LSI composed of the first through the third LSI chips 510 through 512 from its side. The transmitter and receiver circuit 501 is the same as the transmitter and receiver circuit 400 shown in FIG. 4A. The arrow 503 expresses inductive coupling and expresses a state where a plurality of couplings are established in parallel.

[0034]

Further, not only the connection system but also the transmitter and receiver circuit may be altered. Although the power consumption is increased in the transmitter circuit, a configuration depicted in FIG. 6 may be taken if the focus is placed on a decrease in the circuit scale. The transmitter circuit depicted in FIG. 6 is composed of a memory element FF, a transmission buffer INV4 and a voltage source of a bias voltage Vbias. The transmission data Txdata is retained in the memory element FF and is inputted into the transmitter coil L1 via the transmission buffer INV4. The other end of the transmitter

coil L1 is connected to the bias voltage Vbias. If the bias voltage Vbias is set to an intermediate voltage between L and H of the transmission data, any one of positive and negative currents is caused to flow to the transmitter coil L1 at all times. However, the current flowing into the transmitter coil L1 is reversed when the transmission data Txdata changes, and signals are transmitted.

[0035]

In addition, since the receiver circuit is devised so as to receive only the signals for a predetermined cyclic period for which signals are going to be received in synchronization with a receiving clock, noise due to clocks can be removed to increase the SN ratio.

All the publications, patents and patent applications cited in the present specification are taken in the present specification as references.